This listing of claims replaces all prior listings and versions of the claims in the application.

IN THE CLAIMS

1-4. (canceled)

5. (new) A method of generating target instructions from a plurality of first instructions, the target instructions for execution on a target processor, comprising:

automatically analyzing the plurality of first instructions, considered collectively, to determine a purpose to be achieved thereby;

automatically generating the target instructions based on the automatically determined purpose, in preference over particular operations specified by individual ones of the plurality of first instructions.

6. (new) A method as claimed in claim 5, wherein the first instructions are not executable on the first processor.

7. (new) A method for executing target instructions generated according to a method as claimed in claim 5, wherein the purpose is determined and the target instructions are generated at run-time, after accessing the plurality of first instructions from a predetermined memory, the method further comprising executing the target instructions without requiring the target instructions to be first stored to the predetermined memory.

8. (new) A method of generating target instructions as claimed in claim 5, wherein individual ones of the target instructions are generated without regard to particular operations specified by the individual ones of the plurality of first instructions.

9. (new) A method as claimed in claim 5, wherein the plurality of first instructions are according to a first machine language and of a type executable by a first processor but not the target processor, and the target instructions are according to a second machine language and of a type executable by the target processor.

10. (new) A method as claimed in claim 5, wherein the target instructions are generated in a manner to reduce a number of machine cycles required to execute the target instructions.

11. (new) A method as claimed in claim 10, wherein the number of machine cycles is reduced in relation to the number of machine cycles that would be required to execute instructions according to a literal translation of the plurality of first instructions into the second machine language.

12. (new) A method as claimed in claim 9, wherein the target instructions specify a target number of transfers between a register of the target processor and a memory associated with the target processor, the target number being reduced in relation to a number of transfers specified by the plurality of first instructions between a register of the first processor and a memory associated with the first processor.

13. (new) A method as claimed in claim 12, wherein the target number of transfers is further reduced in relation to a number of transfers resulting from a literal translation of the plurality of first instructions into the second machine language.

14. (new) A method as claimed in claim 12, wherein the target instructions are generated so as to minimize the target number of transfers.

15. (new) A method as claimed in claim 12, wherein the number of transfers is further reduced by reducing a number of transfers of a particular operand between the register of the target processor and the memory associated with the target processor, the operand required for execution of each of a plurality of the target instructions.

16. (new) A method as claimed in claim 5, wherein at least one of the target instructions is generated to specify a second physical operation that is different from, but equivalent to a first physical operation specified by one or more instructions of the plurality of first instructions.

17. (new) A method as claimed in claim 16, wherein the at least one target instruction is equivalent in context to the first physical operation.

18. (new) A method as claimed in claim 9, wherein the first processor has a first number of registers and the target processor has a second number of registers which is less than the first number, wherein the target instructions are generated so as to reduce a number of transfers between a register of the target processor and a memory associated with the target processor.

19. (new) A method according to claim 5, wherein the step of generating the target instructions includes eliminating operations specified by the plurality of first instructions which are unnecessary to achieve the determined purpose.

20. (new) A method according to claim 5, further comprising eliminating operations specified by the plurality of first instructions which are unnecessary to support a flow of information to achieve the determined purpose.

21. (new) A method as claimed in claim 5, wherein the step of generating the target instructions includes translating first operations specified by the plurality of first instructions to target operations different from the first operations to reduce the number of machine cycles required to execute the target instructions.

22. (new) A method as claimed in claim 5, wherein the purpose is determined by determining a sequence of operations specified by the plurality of first instructions, removing ones of the specified operations from the sequence which are unnecessary to support the determined purpose, wherein the target instructions are generated after the unnecessary operations are removed from the sequence.

23. (new) A method as claimed in claim 5, wherein a target instruction of the target instructions is generated by selecting an instruction from a plurality of instructions specifying respective equivalent operations, the instruction being selected in a manner to reduce a number of machine cycles required to execute the selected instruction relative to another one of the instructions which specifies the equivalent operation.

24. (new) A machine-readable medium having information recorded thereon for performing a method of generating target instructions from a plurality of first instructions, the target

instructions for execution on a target processor, the method comprising:

automatically analyzing the plurality of first instructions, considered collectively, to determine a purpose to be achieved thereby;

automatically generating the target instructions based on the automatically determined purpose, in preference over particular operations specified by individual ones of the plurality of first instructions.

25. (new) A machine-readable medium as claimed in claim 24, wherein the purpose is determined and the target instructions are generated at run-time, after accessing the plurality of first instructions from a predetermined memory, the method further comprising executing the target instructions without requiring the target instructions to be first stored to the predetermined memory.

26. (new) A machine-readable medium as claimed in claim 24, wherein the plurality of first instructions are according to a first machine language and of a type executable by a first processor but not the target processor, and the target instructions are according to a second machine language and of a type executable by the target processor.

27. (new) A machine-readable medium as claimed in claim 26, wherein the target instructions specify a target number of transfers between a register of the target processor and a memory associated with the target processor, the target number being reduced in relation to a number of transfers specified by the plurality of first instructions between a register of the first processor and a memory associated with the first processor.

28. (new) A machine-readable medium as claimed in claim 27, wherein the number of transfers is further reduced in relation to a number of transfers resulting from a literal translation of the plurality of first instructions into the second machine language.

29. (new) A machine-readable medium as claimed in claim 27, wherein the number of transfers is further reduced by reducing a number of transfers of a particular operand between the register and the memory associated with the target processor, the operand required for execution of each of a plurality of the target instructions.

30. (new) A machine-readable medium according to claim 24, wherein the step of generating the target instructions includes eliminating operations specified by the plurality of first instructions which are unnecessary to achieve the determined purpose.

31. (new) A machine-readable medium as claimed in claim 24, wherein the step of generating the target instructions includes translating first operations specified by the plurality of first instructions to target operations different from the first operations, to reduce the number of machine cycles required to execute the target instructions.

32. (new) A system operable to generate a plurality of target instructions from a plurality of first instructions, the target instructions for execution on a target processor, the system being operable to automatically analyze the plurality of first instructions, considered collectively, to determine a purpose to be achieved thereby, and to automatically generate the target

instructions based on the automatically determined purpose, in preference over particular operations specified by individual ones of the plurality of first instructions.

33. (new) A system as claimed in claim 32, wherein the plurality of first instructions are according to a first machine language and of a type executable by a first processor but not the target processor, and the system is operable to generate the target instructions according to a second machine language and of a type executable by the target processor.

34. (new) A system as claimed in claim 33, wherein the system is operable to generate the target instructions such that, upon execution of the target instructions, a number of transfers between a register of the target processor and a memory associated with the target processor is reduced in relation to the number of transfers specified by the plurality of first instructions between a register of the first processor and a memory associated with the first processor.

35. (new) A system as claimed in claim 34, wherein the system is operable to further reduce the number of transfers between the target processor and the memory associated therewith in relation to a number of transfers resulting from a literal translation of the plurality of first instructions into the second machine language.

36. (new) A system as claimed in claim 34, wherein the system is further operable in relation to transfers specified by the plurality of first instructions, to reduce a number of transfers of a particular operand between the register of the target processor and the memory associated with the target processor,

the operand required for execution of each of a plurality of the target instructions.

37. (new) A system according to claim 32, wherein the system is operable to generate the target instructions so as to eliminate operations specified by the plurality of first instructions which are unnecessary to achieve the determined purpose.

38. (new) A system as claimed in claim 32, wherein the system is operable to generate the target instructions so as to translate first operations specified by the plurality of first instructions to target operations different from the first operations, to reduce a number of machine cycles required to execute the target instructions.

39. (new) A system operable to generate target instructions from a plurality of first instructions, the target instructions for execution by a target processor, the system comprising:

a first stage operable to determine a purpose of the plurality of first instructions, considered collectively, and a first flow of information specified by the plurality of first instructions;

a second stage operable to specify a second flow of information for achieving the determined purpose, in preference over particular operations specified by individual ones of the plurality of first instructions, the second flow of information adapted for more efficient execution on the target processor than the first flow of information; and

a third stage operable to generate target instructions from the second flow of information, the target instructions being executable by the target processor to achieve the determined purpose, wherein the third stage is operable to generate the target instructions through operation including selecting

operation codes of instructions from among a plurality of operation codes specifying different but equivalent physical operations.